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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/995,575	11/29/2001	Tamihide Yasumoto	011317	1497

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EXAMINER	
KIELIN, ERIK J	

ART UNIT	PAPER NUMBER
2813	10

DATE MAILED: 03/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/995,575	Applicant(s) YASUMOTO, TAMIHIDE	
	Examiner Erik Kielin	Art Unit 2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 February 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5 February 2003 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims **1**, 2, 4, 9 and **5**-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6,255,179 B1 (**Cantell** et al.) in view of the excerpt from **Van Zant**, Microchip Fabrication, 4th ed, McGraw-Hill: New York, 2000, pp. 34, 172-173, 179-182.

Regarding claims **1**, 2, and 4, **Cantell** discloses a method of manufacturing a semiconductor device comprising,

forming a wiring comprising silicon on a surface of a semiconductor substrate (col. 5, lines 9-17);

covering part of the wiring with a resist pattern (col. 1, lines 27-38; col. 5, lines 14-15);

implanting ions into the wiring using the resist pattern as a mask (col. 1, lines 27-38; col. 5, lines 14-15);

removing the resist pattern (col. 1, lines 47-52);

thinning the wiring by removing a surface of the wiring to a depth of 10 to 200 Å (1 to 20 nm), more preferably 20-80 Å (2 to 8 nm) to remove the carbon contamination in the silicon wiring generated from "knocked-on carbon from the mask" during the implanting step (col. 4, lines 5-25; col. 5, lines 9-16); and

forming a metal silicide on a surface of the wiring by depositing cobalt or titanium metal on the silicon and then reacting the metal with the silicon by annealing (col. 4, lines 45 to col. 5, line 16),

wherein the wiring thinning step comprises the steps of:

oxidizing the wiring beginning on an upper surface thereof down to a predetermined depth (col. 3, lines 55-57); and

removing an oxidized section of the wiring oxidized in the oxidizing step (col. 4, lines 5-15; col. 5, lines 9-16).

Regarding claims **5**, 6, and 8, **Cantell** discloses a method of manufacturing a semiconductor device comprising,

forming a wiring comprising silicon on a surface of a semiconductor substrate (col. 5, lines 9-17);

covering part of the wiring with a resist pattern (col. 1, lines 27-38; col. 5, lines 14-15);

implanting ions into the wiring using the resist pattern as a mask (col. 1, lines 27-38; col. 5, lines 14-15);

removing the resist pattern (col. 1, lines 47-52);

oxidizing the wiring beginning on an upper surface thereof down to a depth of 10 to 200 Å, more preferably 15-30 Å and (col. 3, lines 55-57);

removing the oxidized portion of the wiring to remove the carbon contamination in the silicon wiring generated from "knocked-on carbon from the mask" during the implanting step (col. 4, lines 5-15; col. 5, lines 9-16); and

forming a metal silicide on a surface of the wiring by depositing cobalt or titanium metal on the silicon and then reacting the metal with the silicon by annealing (col. 4, lines 45 to col. 5, line 16).

As applied to independent claims **1** and **5** above, **Cantell** does not indicate that the implanted ions may be arsenic, but does indicate the n-type dopant is used.

The basic textbook of **Van Zant** teaches that arsenic is a notoriously well-known n-type dopant (p. 34).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use arsenic because **Cantell** states to use an n-type dopant and **Van Zant** teaches that arsenic is an n-type dopant.

Moreover, the selection of a known material based on its suitability for its intended use is *prima facie* obvious. (See MPEP 2144.07.)

As applied to all of the above claims, **Cantell** does not indicate that the apparatus used to oxidize the wiring is a rapid thermal processing apparatus. This limitation is believed to have little patentable weight because it has been held that to be entitled to weight in method claims, the recited structure limitations therein must affect the method in a manipulative sense, and not

amount to the mere claiming of a use of a particular structure. See *Ex parte Pfeiffer*, 1962, C.D. 408 (1961). In the instant case, it appears that the claims merely claim the use of a structure, i.e. the rapid thermal processing apparatus.

If it is thought that the "using a rapid thermal processing apparatus" has patentable weight, and if it is thought that the processing apparatus of **Cantell** is not somehow a rapid thermal processing apparatus, then this may be a difference.

The basic textbook of **Van Zant** teaches that rapid thermal processing is advantageous for reducing thermal budget (p. 180, first sentence).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use a rapid thermal processing apparatus to oxidize the wiring of **Cantell** in order to beneficially reduce the thermal budget.

Regarding claim 7, it is clear that the amount of the silicon oxidized in **Cantell** is less than the depth, otherwise there would be no silicon wiring left, contrary to the teaching in **Cantell**.

Regarding claim 9, **Cantell** does not indicate that a mixture of hydrogen and oxygen is used for the oxidation of the wiring.

Van Zant teaches (p. 181) that rapid thermal oxidation can be carried out using steam, and that steam is beneficially cleaner, and the oxidation process better controlled, by combusting hydrogen and oxygen (paragraph bridging pp. 172-173).

It would have been obvious for one of ordinary skill in the art, at the time of the invention to use an atmosphere of hydrogen and oxygen to form the oxidizing atmosphere, as taught in

Van Zant, to oxidize the wiring of **Cantell,** for at least the better cleanliness and control of the process.

Response to Arguments

4. Applicant's arguments with respect to claims 1, 2, and 4-9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Vines et al. US 6,007,641 teaches that it is known in the art to remove contaminants by oxidizing the silicon substrate and then removing the oxide with entrained contaminants. (See col. 2, lines 4-10; col. 3, lines 1-7.)

Nakanishi et al. US 5,504,022 teaches cleaning a silicon surface by oxidizing the silicon substrate and then removing the oxide. (See col. 3, lines 39-54.)

Kim et al. JP 11-145145 teaches etching back a polysilicon wiring prior to forming a metal silicide thereon. (See Abstract.)

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Erik Kielin whose telephone number is 703-306-5980. The examiner can normally be reached on 9:00 - 19:30 on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached at 703-308-4940. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9318 for regular communications and 703-872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Erik Kielin
March 10, 2003